Remarks

I. DRAWINGS

The applicant respectfully requests the Examiner's approval of the proposed changes indicated in red ink in Figures 1A, 1B, 2A, 2B, 3A and 3B of the drawings. The proposed changes address the objections to the drawings set forth in the Official Action.

II. CLAIMS

A. Thanks

The undersigned attorney thanks Examiner Nguyen for her kind assistance in the course of a telephone interview held on 16 January 2003 in which proposed amendments to the independent claims to address the rejection of claims 1-20 under 35 USC § 112, second paragraph were discussed. The applicant has amended claims 1, 13 and 19 in accordance with the proposed amendments discussed in the telephone interview.

B. Allowable Subject Matter

The applicant notes with appreciation the Examiner's indication that claims 4, 8, 12 and 14 would be allowable if rewritten to overcome the rejections under 35 USC § 112 set forth in the Official Action and to include all of the limitations of the base claims and any intervening claims.

The applicant has amended claims 1 and 13 to incorporate the subject matter claimed in claims 4 and 14, respectively. The applicant has additionally amended claim 1 to address the objection to claim 1 set forth in the Official Action. The applicant has additionally rewritten claim 8 in independent form to incorporate the subject matter claimed in claims 1 and 5 on which claim 8 depends. The applicant has additionally amended claim 12 to make it depend on claim 9, which will be discussed below.

C. Rejection of Claims 1, 9-11, 13 and 18-20 Under 35 USC § 102(b)

Claims 9-11 and 18-20 were rejected under 35 USC § 102(b) as being anticipated by United States Patent No. 4,430,745 of Betts.

The applicant has amended claims 1 and 13 to incorporate the subject matter recited in claims 4 and 14, respectively. The Examiner indicated that claims 4 and 14 would be allowable if rewritten in independent form. Accordingly, the applicant respectfully submits that claims 1 and 13 as now amended are allowable, as the Examiner indicated that claims 4 and 14 were allowable if rewritten in independent form.

The applicant has rewritten claims 9, 18 and 19 in independent form. The applicant has added new independent claim 25 and new dependent claims 21-28 that claim additional subject matter that the applicant believes he is entitled to claim. Claims 10-12 depend on claim 9. New claims 21 and 22 depend on claim 18. Claim 20 and new claims 23 and 24 depend on claim 19. New claims 26-28 depend on new claim 25.

The applicant respectfully submit that claims 9-11 and 18-20 as now amended and new claims 21-28 are patentable because they are not anticipated by Betts. First, Betts fails to disclose "an interleaved clock generator for generating N interleaved clock signals in which N is a non-prime integer", as recited in the independent claims. In Betts' circuit, N=3, which is a prime number.

Second, with reference to claim 9, the applicant respectfully submits that Betts does not disclose "*M* interleaved clock generator means of a second type, each for receiving a respective one of the intermediate clock signals from the clock generator means of the first type and for generating in response thereto N/M of the *N* interleaved clock signals." Each of the element pairs 5 & 7, 33 & 34 and 35 & 36 of Betts' circuit generates only one (N/M=1) of Betts' three (N=3) interleaved clock signals. With the definitions of N and M set forth in claim 9 as now amended, each of the *M* interleaved clock generator means of a second type is recited as generating more than one (N/M>1) of the N (N not prime)

interleaved clock signals. Accordingly, Betts' circuit lacks *M* interleaved clock generator means of a second type as recited in the applicant's claim 9 as now amended. The applicant therefore respectfully submits that his claim 9 as now amended is patentable over Betts.

Third, with reference to claim 18, the applicant respectfully submits that Betts does not disclose "*M* interleaved clock generators of a second type, each including an intermediate clock input connected to a different one of the *M* intermediate clock outputs of the interleaved clock signal generator of the first type, N/M clock outputs and a multi-stage serial-delay circuit, each of the interleaved clock generators of the second type operating in response to the intermediate clock signal to output a respective one of N/M of the interleaved clock signals at each of the clock outputs multi-stage serial-delay circuit." Each of the element pairs 5 & 6, 33 & 34 and 35 & 36 of Betts' circuit generates only one (N/M=1) of Betts' three (N=3) interleaved clock signals. With the definitions of N and M set forth in claim 18 as now amended, each of the *M* interleaved clock generators of a second type is recited as generating more than one (N/M>1) of the N (N not prime) interleaved clock signals. Accordingly, Betts' circuit lacks *M* interleaved clock generators of a second type as recited in the applicant's claim 18 as now amended. The applicant therefore respectfully submits that his claim 18 as now amended is patentable over Betts.

Fourth, with reference to claim 19, the applicant respectfully submits that Betts does not disclose "a multi-stage serial-delay circuit connected to receive the input clock signal, the multi-stage serial-delay circuit including *M* intermediate clock outputs, where M is a factor of N and is an integer greater than unity" as recited in claim 19. None of the element pairs 5 & 6, 33 & 34 and 35 & 36 of Betts' circuit receives the input clock signal TC. Moreover, none of the element pairs 5 & 6, 33 & 34 and 35 & 36 of Betts' circuit generates more than one clock signal and the clock signal generated by these element pairs cannot accurately be called an intermediate clock signal. Accordingly, Betts' circuit lacks a multi-stage

serial-delay circuit as recited in the applicant's claim 19 as now amended. The applicant therefore respectfully submits that his claim 19 as now amended is patentable over Betts.

Fifth, with reference to claim 25, the applicant respectfully submits that Betts does not disclose "connected to each of the *M* intermediate clock outputs, a multi-stage delay circuit that generates N/M of the *N* interleaved clock signals [where *N* is a non-prime integer and *M* is a factor of *N* and is an integer greater than unity]." Each of the element pairs 5 & 6, 33 & 34 and 35 & 36 of Betts' circuit generates only one (N/M=1) of Betts' three (N=3) interleaved clock signals. With the definitions of N and M set forth in claim 25 as now amended, the multi-stage delay circuit connected each of the *M* intermediate clock outputs is recited as generating more than one (N/M>1 of the N (N not prime) interleaved clock signals. Accordingly, Betts' circuit lacks a multi-stage delay circuit as recited in claim 25 connected each of the *M* intermediate clock outputs. The applicant therefore respectfully submits that his claim 25 is patentable over Betts.

The applicant respectfully submits that the claims dependent on claims 9, 18, 19 and 25 are patentable at least because they depend on the respective independent claims.

D. Rejection of Claims 1-3, 5-7, 13 and 15-17 Under 35 USC § 103(a)

Claims 1-3, 5-7, 13, and 15-17 are rejected under 35 USC § 103(a) as being unpatentable over United States Patent No. 6,275,072 of Dally et al. (*Dally*), in view of United States Patent No. 5,268,656 of Muscavage.

The applicant has amended claims 1 and 13 to incorporate the subject matter recited in claims 4 and 14, respectively. The Examiner indicated that claims 4 and 14 would be allowable if rewritten in independent form. Claims 2, 3 and 5-7depend on claim 1. Accordingly, the applicant respectfully submit that claims 2, 3 and 5-7 are also allowable at least because they depend on amended

claim 1. Claims 15-17 depend on claim 13. Accordingly, the applicant respectfully submit that claims 15-17 are also allowable at least because they depend on amended claim 13.

No rejection of claims 9-12 and 18-20 under 35 USC § 103(a) was set forth in the Official Action.

The applicant respectfully requests reconsideration of the rejected claims. The applicant believes that the application as now amended is in condition for allowance, and respectfully requests such favorable action. If any matters remain outstanding in the application, the Examiner is respectfully invited to telephone the applicant's attorney at (650) 485-3015 so that these matters may be resolved.

Respectfully submitted,

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Appendix A

Paper Showing Changes Made to Amended Claims

1. (amended) An interleaved clock generator for generating *N* interleaved clock signals in response to an input clock signal, where *N* is a non-prime integer, the interleaved clock generator comprising:

interleaved clock generator means of a first type for receiving the input clock signal and for generating in response thereto *M* interleaved intermediate clock signals, where *M* is a factor of *N* and is an integer greater than unity, the interleaved clock generator means of the first type including one of (a) a multi-stage serial-delay circuit and (b) a ring counter circuit; and

M interleaved clock generator means of a second type, each for receiving a respective one of the intermediate clock signals from the clock generator means of the first type and for generating in response thereto N/M of the *N* interleaved clock signals, each of the interleaved clock [signal] generator means of the second type including the other of (a) the multi-stage serial-delay circuit and (b) the ring counter circuit, wherein:

corresponding edges of temporally adjacent ones of the interleaved clock signals differ in time by a time delay Td;

the interleaved clock signals have a frequency of 1/(N*Td);

the input clock signal has a frequency of 1/(M*Td) when the interleaved clock generator means of the first type includes the multi-stage serial delay circuit; and

the input clock signal has a frequency of M/(N*Td) when the interleaved clock generator means of the first type includes the ring counter circuit.

8. (amended) An interleaved clock generator for generating *N* interleaved clock signals in response to an input clock signal, where *N* is a non-prime integer, the [The] interleaved clock generator comprising: [of claim 5, in which:]

interleaved clock generator means of a first type for receiving the input clock signal and for generating in response thereto *M* interleaved intermediate clock signals, where *M* is a factor of *N* and is an integer greater than unity, the interleaved clock generator means of the first type including a multi-stage serial-delay circuit; and

M interleaved clock generator means of a second type, each for receiving a respective one of the intermediate clock signals from the clock generator means of the first type and for generating in response thereto N/M of the *N* interleaved clock signals, each of the interleaved clock generator means of the second type including a ring counter circuit, wherein:

the input clock signal comprises differential clock signals each having a 50% duty cycle; and

the multi-stage serial-delay circuit includes M/2 delay stages, each providing two of the intermediate clock signals.

9. (amended) An interleaved clock generator for generating *N* interleaved clock signals in response to an input clock signal, where *N* is a non-prime integer, the [The] interleaved clock generator comprising: [of claim 1, in which:]

interleaved clock generator means of a first type for receiving the input clock signal and for generating in response thereto *M* interleaved intermediate clock signals, where *M* is a factor of *N* and is an integer greater than unity, the interleaved clock generator means of the first type including a [includes the] ring counter circuit; and

M interleaved clock generator means of a second type, each for receiving a respective one of the intermediate clock signals from the clock generator means of the first type and for generating in response thereto N/M of the *N* interleaved clock signals, each of the interleaved clock signal generator means of the second type including a [includes the] multi-stage serial-delay circuit.

12. (amended) The interleaved clock generator of claim 9, [5,] in which:

each intermediate clock signal comprises differential clock signals each having a 50% duty cycle; and

the multi-stage serial-delay circuit includes N/2M delay stages, each providing two of the interleaved clock signals.

13. (amended) An interleaved clock generator for generating *N* interleaved clock signals in response to an input clock signal, where *N* is a non-prime integer, the interleaved clock generator comprising:

an interleaved clock generator of a first type, including a clock input connected to receive the input clock signal, *M* intermediate clock outputs, where *M* is a factor of *N* and is an integer greater than unity, and one of (a) a multi-stage serial-delay circuit and (b) a ring counter circuit, the interleaved clock generator of the first type operating in response to the input clock signal to output a respective intermediate clock signal at each of the intermediate clock outputs; and

M interleaved clock generators of a second type, each including an intermediate clock input connected to a different one of the *M* intermediate clock outputs of the interleaved clock signal generator of the first type, N/M clock outputs and the other of (a) the multi-stage serial-delay circuit and (b) the ring counter circuit, each of the interleaved clock generators of the second type operating in response to the intermediate clock signal to output a respective one of N/M of the interleaved clock signals at each of the clock outputs, wherein:

corresponding edges of temporally adjacent ones of the interleaved clock signals differ in time by a time delay Td;

the interleaved clock signals have a frequency of 1/(N×Td);

the input clock signal has a frequency of 1/(M×Td) when the interleaved clock generator of the first type includes the multi-stage serial delay circuit;

the input clock signal has a frequency of M/(N×Td) when the interleaved clock generator of the first type includes the ring counter circuit.

18. (amended) An interleaved clock generator for generating *N* interleaved clock signals in response to an input clock signal, where *N* is a non-prime integer, the [The] interleaved clock generator comprising: [of claim 13, in which:]

an [the] interleaved clock generator of a first type, including a clock input connected to receive the input clock signal, *M* intermediate clock outputs, where *M* is a factor of *N* and is an integer greater than unity, and [includes] a ring counter circuit, the interleaved clock generator of the first type operating in response to the input clock signal to output a respective intermediate clock signal at each of the intermediate clock outputs; and

M interleaved clock generators of a second type, each including an intermediate clock input connected to a different one of the *M* intermediate clock outputs of the interleaved clock signal generator of the first type, N/M clock outputs and a [each of the interleaved clock signal generators of the second type includes the] multi-stage serial-delay circuit, each of the interleaved clock generators of the second type operating in response to the intermediate clock signal to output a respective one of N/M of the interleaved clock signals at each of the clock outputs multi-stage serial-delay circuit.

21. (new) The interleaved clock generator of claim 18, in which:

corresponding edges of temporally-adjacent ones of the interleaved clock signals differ in time by a time delay Td;

the interleaved clock signals have a frequency of 1/(N×Td); and

the input clock signal has a frequency of M/(N×Td).

22. (new) The interleaved clock generator of claim 18, in which:

each intermediate clock signal comprises differential clock signals each having a 50% duty cycle; and

the multi-stage serial-delay circuit includes N/2M delay stages, each providing two of the interleaved clock signals.

19. (amended) An interleaved clock generator for generating *N* interleaved clock signals in response to an input clock signal, where *N* is a non-prime integer, the interleaved clock generator comprising:

a multi-stage serial-delay circuit connected to receive the input clock signal, the multi-stage serial-delay circuit including *M* intermediate clock outputs where *M* is a factor of *N* and is an integer greater than unity; and

connected to each of the *M* intermediate clock outputs, a ring counter circuit that generates N/M of the *N* interleaved clock signals.

23. (new) The interleaved clock generator of claim 19, in which:

corresponding edges of temporally-adjacent ones of the interleaved clock signals differ in time by a time delay Td;

the interleaved clock signals have a frequency of 1/(N×Td); and

the input clock signal has a frequency of 1/(M×Td).

24. (new) The interleaved clock generator of claim 19, in which:

each intermediate clock signal comprises differential clock signals each having a 50% duty cycle; and

the multi-stage serial-delay circuit includes M/2 delay stages, each providing two of the intermediate clock signals.

25. (new) An interleaved clock generator for generating *N* interleaved clock signals in response to an input clock signal, where *N* is a non-prime integer, the interleaved clock generator comprising:

a ring counter circuit connected to receive the input clock signal, the ring counter circuit including *M* intermediate clock outputs, where *M* is a factor of *N* and is an integer greater than unity; and

connected to each of the *M* intermediate clock outputs, a multi-stage delay circuit that generates N/M of the *N* interleaved clock signals.

26. (new) The interleaved clock generator of claim 25, in which the ring counter circuit comprises an M-stage ring counter.

27. (new) The interleaved clock generator of claim 25, in which:

corresponding edges of temporally-adjacent ones of the interleaved clock signals differ in time by a time delay Td;

the interleaved clock signals have a frequency of 1/(N×Td); and

the input clock signal has a frequency of M/(N×Td).

28. (new) The interleaved clock generator of claim 25, in which:

each intermediate clock signal comprises differential clock signals each having a 50% duty cycle; and

the multi-stage serial-delay circuit includes N/2M delay stages, each providing two of the interleaved clock signals.